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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/534,190	05/06/2005	Shuichi Kawasaki	1217-051112	5305

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EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	**PAPER NUMBER**
2841	

MAIL DATE	DELIVERY MODE
07/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/534,190	KAWASAKI, SHUICHI	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *1-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/19 and 1/3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of specie A1B1, claims 1-16 in the reply filed on July 5, 2007 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been received and placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement filed on October 19, 2005 is partly considered. Copy of four of the Japanese art not found in the file on record. Applicant is request to submit the copies.

Specification

4. The abstract of the disclosure is objected to because of the presence of the legal phraseology "comprising". It may be replace by having or including.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-6, 8-13 and 15-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Masahiko Saeki (Japanese Patent No. JP404365343A).

Regarding claim 1, Masahiko in figure 1 discloses a film carrier tape for mounting an electronic part, comprising an elongated insulating film (1) having a plurality of wiring patterns (eight areas of wiring pattern, see abstract) formed on a surface of the insulating film, said wiring patterns being made of a conductive metal (copper), wherein: the wiring patterns are each independently covered with a solder resist layer (8) except a connecting terminal portion (inner lead region and outer lead region are exposed), and the solder resist layer formed on each surface of the wiring patterns is divided into plural sections (see figure).

Regarding claim 2, Masahiko in figure 1 discloses film carrier tape for mounting an electronic part, comprising an elongated insulating film (1) having a plurality of wiring patterns (eight areas of wiring pattern) formed on a surface of the insulating film, said wiring patterns being made of a conductive metal (copper) and at least two of said wiring patterns being arranged side by side in the width direction (see figure) of the

elongated insulating film, wherein: the wiring patterns are each independently covered with a solder resist layer (8) except a connecting terminal portion (inner lead region and outer lead region are exposed), and the solder resist layer formed on each surface of the wiring patterns is divided into plural sections (see figure).

Regarding claim 3, Masahiko further discloses the solder resist layer is formed on each surface of the wiring patterns in such a manner that the solder resist layer is divided into 2 to 16 sections (eight parts, see abstract and figure).

Regarding claim 4, Masahiko further discloses a distance between one section and its adjacent section of the divided solder resist layer is in the range of 20 μm to 50 mm (as the width of the film is 35 μm, the distance between the adjacent section is less than 35 mm, column 2, line 7, as translated by the translator).

Regarding claim 5, Masahiko further discloses the elongated insulating film has a thickness of not more than 75 μm (50 μm, column 2, line 7, as translated by the translator).

Regarding claim 6, Masahiko further discloses an area occupied by one film carrier is substantially the same as an area of an electronic part (device to be mounted in device hole 2) to be mounted on the film carrier tape.

Regarding claim 8, Masahiko further discloses the solder resist layer formed on the surface of the wiring pattern has an average thickness, except non-solder resist area, of 3 to 50 μm after curing (20 μm, column 2, line 10, as translated by the translator).

Regarding claim 9, Masahiko further discloses the solder resist layer is formed in a region of not less than 20% of the wiring patterns except the connecting terminal portions (see figure, as only inner and outer lead regions are exposed, the solder resist area is much more than 20 % of the wiring pattern).

Regarding claim 10, Masahiko further discloses the solder resist layer is formed on each surface of the wiring patterns in such a manner that the solder resist layer is divided into 2 to 16 sections (eight section, see abstract and figure).

Regarding claim 11, Masahiko further discloses a distance between one section and its adjacent section of the divided solder resist layer is in the range of 20 μm to 50 mm (as the width of the film is 35 μm, the distance between the adjacent section is less than 35 mm, column 2, line 7, as translated by the translator).

Regarding claim 12, Masahiko further discloses the elongated insulating film has a thickness of not more than 75 μm (50 μm, column 2, line 7, as translated by the translator).

Regarding claim 13, Masahiko further discloses an area occupied by one film carrier is substantially the same as an area of an electronic part (device to be mounted in device hole 2) to be mounted on the film carrier tape.

Regarding claim 15, Masahiko further discloses the solder resist layer formed on the surface of the wiring pattern has an average thickness, except non-solder resist area, of 3 to 50 μm after curing (20 μm, column 2, line 10, as translated by the translator).

Regarding claim 16, Masahiko further discloses the solder resist layer is formed in a region of not less than 20% of the wiring patterns except the connecting terminal portions (see figure, as only inner and outer lead regions are exposed, the solder resist area is much more than 20 % of the wiring pattern).

Claim Rejections - 35 USC § 103

7. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masahiko as applied to claims 1 and 2 above, and further in view of Kaneda (US Patent No. 7,211,735).

Regarding claims 7 and 14, Masahiko discloses all the features of the claimed invention as applied to claims 1 and 2 respectively but does not disclose an opposite surface to the surface of the insulating film where the wiring pattern of the film carrier for

mounting an electronic part is formed is designed so that metal balls to be electrically connected outside the film carrier can be arranged. However, forming metal balls / bumps is old and known in the art. Kneda disclose a film like substrate 2 with wiring pattern (3) on one side and metal bump (11) for external connection.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the film carrier of Masahiko with the opposite surface to the surface of the insulating film where the wiring pattern of the film carrier for mounting an electronic part is formed designed so that metal balls to be electrically connected outside the film carrier can be arranged as recited in claims 7 and 14, as taught by kaneda, in order to facilitate external connection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cho (US Patent No. 6,914,196) in figure (9) discloses a flexible board (68) with plurality of unit board (60) formed on the substrate.

Saito (US Patent No. 6,320,135) in figure (10) discloses a base film (101) with solder mask coating (118) except input out put wires (112a and 112b).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on (571) 272 1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IBPatel

Ishwar (I. B.) Patel
Primary Examiner
Art Unit: 2841

ibp
July 23, 2007